Client's ref. :TSMC2003-0866
Our ref: 0503-9728-US/final/Cherry

TITLE

BONDING PAD STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to integrated circuits, and more particularly to a bonding pad structure.

Description of the Related Art:

Bonding pads are interfaces between integrated circuits contained in semiconductor chips and a device package. Modern IC designs with high circuit density require a significantly increased number of pins and bonding pads to reduce bonding pad pitch and size. Large mechanical stresses inherent in bonding operations, however, easily damage smaller bonding pads.

Traditionally, each bonding pad is connected to one or more contact pads on an IC-mounting surface of the device package through wire-bonding, tape automated bonding (TAB) or flip-chip technologies. When an IC chip is probed in an electrical test or the like, a probe pin may damage the soft surface of the bonding pad. The Cu layer beneath the AlCu pad is exposed to air, and may be corroded. The corroded pads caused by this type of pad voids degrade the bondability of wire connection. Currently, a top copper layer of a solid profile is used for connecting an aluminum pad, but has disadvantages of pad voids, narrow bondability window, ball lifting and dielectric crack issues. Accordingly, several modifications of the top copper layer have been developed as listed below. Moreover, in order to

overcome this problem, the bonding pad has been divided into a bonding pad region and a sensing pad region, and the probe pin is brought into contact only with the sensing pad region which is allowed to be damaged.

As disclosed in US Patent No.6,552,438, one conventional bonding pad comprises a plurality of independent metal plugs formed in an array of via holes of an inter-dielectric layer, in which each metal plug has a bottom portion connected to a lower aluminum layer and a top portion connected to an upper aluminum pad. Moreover, a passivation layer is formed on the aluminum pad to expose a predetermined bonding area for bonding a wire. Another conventional bonding pad comprises a top metal layer filling a lattice trench of an inter-dielectric layer for surrounding dielectric islands. A passivation layer is also formed on the top metal layer to expose a predetermined bonding area for forming an aluminum pad, thus allowing a ball to be bonded on the aluminum pad.

The above-described bonding pads, however, have the following disadvantages. During wafer sorting, wire bonding or probe pin testing, applied forces or large mechanical stresses may crack the inter-dielectric layer adjacent to a probe pin region. Second, the crack may extend into the interior of the inter-dielectric layer surrounding the top metal layer, causing corrosion and layer-open problems. This also causes the aluminum pad to peel from the top metal layer, thus the pad-open problem causes the wire to lose contact with the aluminum pad, decreasing bonding reliability. Additionally, the pitch and size of the bonding pad cannot be further shrinked as the bonding pad is

susceptible to damage from the mechanical stress, thus limiting chip size reduction in next generation technologies. Fourth, during wire bonding, a high distribution ratio of the independent metal plugs or the dielectric islands may create a pad finding issue.

As disclosed in US Patent No.6,566,752, another conventional bonding pad comprises a top metal ring formed in a trench of an inter-dielectric layer. A passivation layer with a plurality of via holes is formed on the inter-dielectric layer to expose the top metal ring. An aluminum pad is formed on the passivation layer and is electrically connected to the top metal ring through via holes. However, the width of the top metal ring is limited by the via hole design, resulting in a misalignment problem during photolithography, which prohibits bonding pad fabrication within active areas.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a top metal layer design for a bonding pad structure to obtain a metal-free area or a small metal area under a metal pad within a sensing region.

According to the object of the invention, a bonding pad structure comprises a substrate having a bonding region and a sensing region. A first dielectric layer is formed overlying the substrate and has a dielectric island surrounded by a ring-shaped trench. A first conductive layer is formed in the ring-shaped trench of the first dielectric layer. A passivation layer is formed overlying the first dielectric layer and has an opening, in which the

opening corresponds to the bonding region and the sensing region and exposes the dielectric island and a part of the first conductive layer. A second conductive layer covers the opening of the passivation layer and is electrically connected to the first conductive layer.

Another object of the present invention is to provide a passivation opening design for a bonding pad structure to protect a top metal layer under a metal pad within a sensing region.

According to the object of the invention, a bonding pad structure comprises a substrate having a bonding region and a sensing region. A first dielectric layer is formed overlying the substrate and has a trench. A first conductive layer is formed in the trench of the first dielectric layer. A passivation layer is formed overlying the first dielectric layer and has an opening corresponding to the bonding region, wherein the passivation layer covers the first conductive layer formed within the sensing region. A second conductive layer covers the opening of the passivation layer and is formed overlying the sensing region. The second conductive layer is electrically connected to the first conductive layer.

DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIG. 1 is a top view of an individual chip including bonding pad structures of the present invention.

FIG. 2A is a cross-section of a bonding pad structure according to the first embodiment of the present invention.

FIG. 2B is a top view of the conductive ring shown in FIG. 2A.

FIG. 3A is a cross-section of another conductive ring underlying the conductive ring.

FIG. 3B is a cross-section of a conductive lattice underlying the conductive ring.

FIG. 3C is a cross-section illustrating a conductive solid underlying the conductive ring.

FIGS. 4A~4F are top views illustrating examples of profile designs for the conductive ring.

FIGS. 5A~5F are top views illustrating examples of the profile designs for the conductive pad.

FIG. 6A is a top view of corner cut portions of the conductive ring.

FIG. 6B is a top view of corner cut portions of the conductive pad.

FIG. 7A is a top view of the conductive ring with a marking notch.

FIG. 7B is a top view of the conductive pad with a marking notch.

FIG. 8A is a top view of the conductive ring with the marking notches and the corner cut portions.

FIG. 8B is a top view of the conductive pad with the marking notches and the corner cut portions.

FIG. 9A is a cross-section of a CUP scheme adjacent to the bonding pad structure.

FIG. 9B is a top view of the conductive ring and the CUP scheme shown in FIG. 9A.

FIG. 10A is a cross-section of one example of forming the CUP scheme without using the buffer layer.

FIG. 11A is a cross-section of a bonding pad structure according to the second embodiment of the present invention.

FIG. 11B is a top view of the conductive ring and the passivation layer shown in FIG. 11A.

FIG. 12A is a cross-section of the first conductive layer patterned as a lattice.

FIG. 12B is a top view of the conductive layer shown in FIG. 12A.

FIG. 13A is a cross-section of the first conductive layer patterned as independent plugs.

FIG. 13B is a top view of the conductive layer shown in FIG. 13A.

FIG. 14A is a cross-section of the first conductive layer patterned as a solid form.

FIG. 14B is a top view of the conductive layer shown in FIG. 14A.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a top metal layer design for a bonding pad structure to obtain a metal-free area or a small metal area under a metal pad within a sensing region. The present invention additionally provides a passivation opening design for a bonding pad structure to protect a top metal layer under a metal pad within a sensing region. The present invention effectively prevents corrosion in the top metal layer due to probing, lengthens the bondability window, eliminates cracks in the under-layer dielectrics, and prevents peeling of the metal pad from the under-layer dielectrics. The present invention also improves pad finding capability (pad recognition capability), reduces pad pitch, and allows the bonding pad structures to be located over peripheral circuit areas, active areas, scribe lines or a combination thereof.

FIG. 1 is a top view of an individual chip including bonding pad structures of the present invention. A semiconductor wafer comprises substantially isolated chips, and the isolated chip comprises a main area 10 defined by first scribe lines 12 extending in a first direction and second scribe lines 14 extending in a second direction. The individual chip 10 containing circuitry comprises an active area 16 and a peripheral area 18. A plurality of bonding structures 20 is allowed on the active area 16, the peripheral area 18, the first scribe line 12, the second scribe line 14, or a combination thereof. The bonding pad structures 20 may be aligned in a single line or staggered to form CUP (circuit under pad) pads.

The bonding pad structures 20 with a top metal layer design and a passivation opening design for obtaining a metal-free area or a small metal area under a metal pad within a sensing region are described below.

First Embodiment

The present invention provides a bonding pad structure with a top metal layer design for obtaining a metal-free area or a small metal area under a metal pad within a sensing region.

FIG. 2A is a cross-section of a bonding pad structure according to the first embodiment of the present invention. FIG. 2B is a top view of the conductive ring shown in FIG. 2A.

A semiconductor substrate 22 with partially completed integrated circuits has a bonding region I for bonding a ball or a bump and a sensing region II for testing by probe pins or other implement. A first dielectric layer 24, an next level dielectric of the substrate 22, comprises a ring-shaped trench 25 which correspondingly defines a dielectric island 24a. A first conductive layer 26, an uppermost interconnection of the substrate 22, fills the ring-shaped trench 25 to serve as a conductive ring 26, thus enclosing the dielectric island 24a. A passivation layer 30 is formed on the first dielectric layer 24, and has an opening 31 corresponding to the bonding region I and the sensing region II, thus exposing the dielectric island 24a and a sufficient area of the conductive ring 26. A second conductive layer 32 is patterned on the first dielectric layer 24 and the passivation layer 30 within the bonding region I and the sensing region II to serve as a conductive pad 32, in which

the conductive pad 32 is directly connected to the conductive ring 26 without requiring via holes. A bonding element 34, such as a ball or a bump, is bonded on the conductive pad 32 within the bonding region I. Moreover, a barrier layer 28 is formed on an interface between the conductive pad 32 and the conductive ring 26 for increasing adhesion therebetween.

The first dielectric layer 24 may be plasma oxide, HDP (high density plasma) oxide, dielectric with high resistance to mechanical stress, low-k dielectrics, fluorinated silicate glass (FSG) or silicon-based dielectrics. The conductive ring 26 may be copper (Cu), aluminum (Al), AlCu alloy, a copper manganese alloy or a copper-containing alloy. The conductive ring 26 is approximately 1~50 μm in width and 0.5~2μm in depth. Preferably, a measurement ratio R_1 satisfies the formula: $R_1 = A_r/A_s$ and $0 \le R_1 \le 30\%$, where A_r is the area of the conductive ring 26 formed within the sensing region II, and A_s is the area of the sensing region II. The barrier layer 28 may be Ti, TiN, W, WN, Ta, TaN, or a combination thereof. The conductive pad 32 may be aluminum (Al), AlCu alloy or an aluminum-containing alloy. The bonding element 34 may be a gold ball used in wire bonding technology or a metal bump used in a flip chip technology.

In accordance with the top metal layer design, the conductive ring 26 occupies a small area of the sensing region II to achieve a metal-free area or a small metal area, thus overcoming problems caused by the conventional bonding pads and obtains the following advantages. The metal-free area or the small metal area effectively reduces

the possibility of cracks penetrating the first dielectric layer 24 to the conductive ring 26, thus preventing corrosion and layer-open problems. The metal-free or small metal area prevents peeling of the conductive pad 32 from the conductive ring 26 or the first dielectric layer 24, thus eliminating pad-open problems and ensuring bonding reliability. Additionally, the pitch and size of the bonding pad structure 20 can be further reduced since the conductive ring 26 is not susceptible to damage from mechanical stress, thus allowing reduction in chip size for next generation technologies. The pad finding capability of the wire bonding tool is effectively improved as only one smooth dielectric island 24a is enclosed by the conductive ring 26. Finally, since the conductive ring 26 is directly connected to the conductive pad 32 without use of via holes or plugs, limitation in ring width and misalignment problems caused by a via hole design are eliminated, and various modifications of the conductive ring 26 and the conductive pad 32 are allowed.

Various modifications of the conductive ring 26 and the conductive pad 32 are herein described.

First Example

Based on design requirements of the top metal layer, the interconnections underlying the conductive ring 26 may be modified to have a ring, lattice, island, or solid profile.

FIG. 3A is a cross-section of another conductive ring underlying the conductive ring 26. Elements similar to those in FIG. 2A are omitted here. A second dielectric layer 36 underlying the first dielectric layer 24 is

provided. A third conductive layer 38 is patterned as a ring and embedded in the second dielectric layer 36. A conductive plug 40 is also formed in the second dielectric layer 36 to electrically connect the conductive ring 26 to the second conductive layer 38.

FIG. 3B is a cross-section of a conductive lattice underlying the conductive ring 26. Elements similar to those in FIG. 3A are omitted here. The third conductive layer 38 is modified to form a lattice, in which an array of dielectric islands 36a is provided and the dielectric islands 36 are spaced apart from each other by the third conductive layer 38. Alternately, the third conductive layer 38 is modified to form an array of independent plugs spaced apart from each other by the second dielectric layer 36.

FIG. 3C is a cross-section illustrating a conductive solid underlying the conductive ring 26. Elements similar to those in FIG. 3A are omitted here. The third conductive layer 38 is modified to have a solid form.

Second Example

Based on the design requirements of the top metal layer, the conductive ring 26, the conductive pad 32, or a combination thereof may be further modified to have various geometric shapes.

FIGS. 4A~4F are top views illustrating examples of profile designs for the conductive ring 26. FIGS. 5A~5F are top views illustrating examples of the profile designs for the conductive pad 32.

The conductive ring 26 is a quadrilateral ring, and the corresponding dielectric island 24a is a quadrilateral

solid. In FIG. 4A, the conductive ring 26 is a square ring, and the corresponding dielectric island 24a is a square solid. In FIG. 4B, the conductive ring 26 is a rectangular ring, and the corresponding dielectric island 24a is a rectangular solid.

The conductive ring 26 is a circular ring, and the corresponding dielectric island 24a is a circular solid. In FIG. 4C, the conductive ring 26 is a circular ring, and the corresponding dielectric island 24a is a circular solid. In FIG. 4D, the conductive ring 26 is an elliptical ring, and the corresponding dielectric island 24a is an elliptical solid.

The conductive ring 26 is a polygonal ring, and the corresponding dielectric island 24a is a polygonal solid. In FIG. 4E, the conductive ring 26 is a hexagonal ring, and the corresponding dielectric island 24a is a hexagonal solid. In FIG. 4F, the conductive ring 26 is an octagonal ring, and the corresponding dielectric island 24a is an octagonal solid.

The conductive pad 32 may only be shaped into a geometric solid if the electrical connection between the conductive pad 32 and the conductive ring 26 is reliable. In FIG. 5A, the conductive pad 32 is a square solid. In FIG. 5B, the conductive pad 32 is a rectangular solid. In FIG. 5C, the conductive pad 32 is a circular solid. In FIG. 5D, the conductive pad 32 is an elliptical solid. In FIG. 5E, the conductive pad 32 is a hexagonal solid. In FIG. 5F, the conductive pad 32 is an octagonal solid.

Third Example

Based on a quadrilateral design for the conductive ring 26 or the conductive pad 32, at least one corner cut portion is provided to prevent peeling.

FIG. 6A is a top view of corner cut portions of the conductive ring 26. FIG. 6B is a top view of corner cut portions of the conductive pad 32. Elements similar to those in FIG. 2B are omitted here.

In FIG. 6A, the conductive ring 26 comprises four corner cut portions 42 adjacent to four corners of the quadrilateral ring, respectively. The corner cut portion 42 prohibits the formation of the first conductive layer 26, but allows the formation of the first dielectric layer 24. Preferably, the corner cut portion 42 is a right triangle, where the hypotenuse 41 is approximately 0.5~5μm in length, an included angle θ_1 between the hypotenuse 41 and the X axis is approximately 10°~80°, and a measurement ratio R_2 satisfies the formula: $R_2= A_{t1}/A_{c1}$ and $0<R_2<80\%$, where A_{t1} is the area of the corner cut portion 42, and A_{c1} is the corner area of the conductive ring 26. The corner area A_{c1} satisfies the formula: $A_{c1}=W_1 \times W_2$, where W_1 is the X-axis width of the conductive ring 26, W_2 is the Y-axis width of the conductive ring 26, W_1=1μm ~10μm, and W_2=1μm~10μm.

In FIG. 6B, the conductive pad 32 comprises four corner cut portions 44 adjacent to four corners of the quadrilateral solid, respectively. The corner cut portion 44 prohibits the formation of the second conductive layer 32, but allows the formation of the passivation layer 30. Preferably, the corner cut portion 44 is a right triangle, where the hypotenuse 43 is approximately 0.5~10μm in length,

and an included angle θ_2 between the hypotenuse 41 and the X axis is approximately 10°~80°.

Fourth Example

In order to clearly discriminate the sensing region II from the bonding region I, a marking notch is provided on the conductive ring 26, the conductive pad 32, or a combination thereof.

FIG. 7A is a top view of the conductive ring 26 with a marking notch. FIG. 7B is a top view of the conductive pad 32 with a marking notch. Elements similar to those in FIG. 2B are omitted here.

In FIG. 7A, the conductive ring 26 comprises two marking notches 46, and two dielectric markings 24b are correspondingly defined within the two marking notches 46, respectively. The two marking notches 46 are approximately aligned in a line to delineate the sensing region II from the bonding region I. Each of the two marking notches 46 is composed of a bottom side 46I and two lateral sides 46II. Preferably, a first-direction length L_1 from the lateral side 46II to the edge of the conductive ring 26 for defining the bonding region I is approximately 40~60μm. Preferably, a first length S_1 of the dielectric marking 24b, parallel to the bottom side 46I, is approximately 1~3μm. Preferably, a second length S_2 of the dielectric marking 24b, parallel to the lateral side 46II, is approximately 0.5~2μm.

In FIG. 7B, the conductive pad 32 comprises two marking notches 48, and two passivation markings 30b are correspondingly defined within the two marking notches 48, respectively. The two marking notches 48 are approximately aligned in a line to delineate the sensing region II from

the bonding region I. Each of the two marking notches 48 is composed of a bottom side 48I and two lateral sides 48II. Preferably, a first-direction length L_1 from the lateral side 48II to the edge of the conductive pad 32 for defining the bonding region I is approximately 40~60μm. Preferably, a first length S_1 of the passivation marking 30b, parallel to the bottom side 48I, is approximately 1~3μm. Preferably, a second length S_2 of the passivation marking 30b, parallel to the lateral side 48II, is approximately 0.5~2μm.

Additionally, the marking notch design for the conductive ring 26 and the conductive pad 32 can be combined with the corner cut designs as described in FIGS. 6A and 6B.

FIG. 8A is a top view of the conductive ring 26 with the marking notches 46 and the corner cut portions 42. FIG. 8B is a top view of the conductive pad 32 with the marking notches 48 and the corner cut portions 44. Elements similar to those in FIGS. 6~7 are omitted here.

Fifth Example

Based on the design requirements of the top metal layer, a circuit under pad (CUP) scheme can be further provided under an extension portion the conductive ring 26. Locating the circuit under the pad shortens some of the conductors and thereby decreases their inductance and resistance and also reduces the parasitic capacitance of the circuit.

FIG. 9A is a cross-section of a CUP scheme 50 adjacent to the bonding pad structure 20. FIG. 9B is a top view of the conductive ring 26 and the CUP scheme 50 shown in FIG. 9A. Elements similar to those in FIGS. 6~7 are omitted here.

The conductive ring 26 comprises an extension portion 26a which extends from one peripheral edge of the conductive ring 26 and away from the bonding region I and the sensing region II. A CUP scheme 50 is formed adjacent to the extension portion 26a. A buffer layer 52 is formed underneath the first dielectric layer 24 and has a circuit scheme 54 patterned therein. A plurality of conductive plugs 56 is formed in an array of via holes 57 of the first dielectric layer 24. Thus, the extension portion 26a can be electrically connected to the circuit scheme 54 through via holes 57. Also, the circuit scheme 54 can be electrically connected to a lowermost conductive layer 58 through interconnections. Preferably, the number of via holes 57 for a signal circuit scheme is smaller than that for a power circuit scheme.

In addition, based on a combination of the conductive ring 26 and the CUP scheme 50, the buffer layer 52 may be optional, and the conductive layers underlying the conductive ring 26 may be modified.

FIG. 10A is a cross-section of one example of forming the CUP scheme 50 without using the buffer layer 52. Elements similar to those in FIG. 9A are omitted here. The different portion is that the buffer layer 52 is omitted, thus the circuit scheme 54 is formed in the first dielectric layer 24.

FIG. 10B is a cross-section of another example of forming the CUP scheme 50 underneath two conductive rings. Elements similar to those in FIG. 9A are omitted here. The different portion is that the third conductive layer 38 is patterned as a ring and embedded in the second dielectric

layer 36, and is electrically connected to the conductive ring 26 through the conductive plug 40. Also, the third conductive layer 38 has an extension portion 38a which extends from one peripheral edge of the ring to be electrically connected to the circuit scheme 54 through via holes 57.

Second Embodiment

The present invention provides a bonding pad structure with a passivation opening design for protecting a top metal layer within a sensing region.

FIG. 11A is a cross-section of a bonding pad structure according to the second embodiment of the present invention. FIG. 11B is a top view of the conductive ring 26 and the passivation layer 30 shown in FIG. 11A.

A semiconductor substrate 22 with partially completed integrated circuits has a bonding region I for bonding a ball or a bump and a sensing region II for testing by probe pins or other implement. A first dielectric layer 24, an uppermost dielectric of the substrate 22, comprises a ring-shaped trench 25 which correspondingly defines a dielectric island 24a. A first conductive layer 26, an uppermost conductive layer of interconnections in the substrate 22, fills the ring-shaped trench 25 to serve as a conductive ring 26, thus enclosing the dielectric island 24a. A passivation layer 30 is formed on the first dielectric layer 24, and has an opening 31 corresponding to the bonding region I, thus covering the conductive ring 26 located within the sensing region II. A second conductive layer 32 is formed overlying the first dielectric layer 24 and the passivation layer 30 within the bonding region I and the

sensing region II to serve as a conductive pad 32, in which the conductive pad 32 is directly connected to the conductive ring 26 without requiring via holes. A bonding element 34, such as a ball or a bump, is bonded to the conductive pad 32 within the bonding region I. Moreover, a barrier layer 28 is provided on an interface between the conductive pad 32 and the conductive ring 26.

Preferably, the first dielectric layer 24 may be plasma oxide, HDP (high density plasma) oxide, dielectric with high resistance to mechanical stress, low-k dielectrics, FSG, or silicon-based dielectrics. The conductive ring 26 may be copper (Cu), aluminum (Al), AlCu alloy, a copper manganese alloy or a copper-containing alloy. The conductive ring 26 is approximately 1~50μm in width and 0.5~2μm in depth. The barrier layer 28 may be Ti, TiN, W, WN, Ta, TaN, or a combination thereof. The conductive pad 32 may be aluminum (Al), AlCu alloy or an aluminum-containing alloy. The bonding element 34 may be a gold ball used in wire bonding technology or a metal bump used in a flip chip technology.

Accordingly, the passivation layer 30 covers the conductive ring 26 within the sensing region II to prevent damage to the conductive ring 26 within the sensing region caused by mechanical stress. The passivation layer 30 adjacent to the demarcation between the bonding region I and the sensing region II can also serve as a marking strip, which has the same function of the marking notches as described in FIGS. 7A and 7B. In addition, other interconnections underlying the conductive ring 26 may be modified to have a ring, lattice, island, or solid profile as disclosed in FIGS. 3A~3C.

The passivation opening design for the passivation layer 30 achieves the following advantages. The passivation layer 30 covers the conductive ring 26 within the sensing region II to prohibit dielectric cracks from penetrating into the conductive ring 26, thus preventing corrosion and layer-open problems. The passivation layer also prevents peeling of the conductive pad 32 from the conductive ring 26 or the first dielectric layer 24, thus eliminating a pad-open problem and ensuring bonding reliability. The pitch and size of the bonding pad structure 20 can be further reduced since the conductive ring 26 is not susceptible to damage from mechanical stress, thus allowing chip size reduction for next generation technologies. The pad finding capability can be effectively improved during wire bonding as only one dielectric island 24a is enclosed by the conductive ring 26,. Finally, the conductive ring 26 is directly connected to the conductive pad 32 without use of via holes or plugs, thus limitation in ring width and misalignment problems caused by via hole design are eliminated, enabling various modifications of the conductive ring 26 and the conductive pad 32.

Various modifications of the conductive ring 26 and the conductive pad 32 are herein described.

First Example

Based on the passivation opening design rule, the first conductive layer 26 may be further modified to have a lattice form or as independent plugs.

FIG. 12A is a cross-section of the first conductive layer 26 patterned as a lattice form. FIG. 12B is a top view of the first conductive layer 26 shown in FIG. 12A.

Elements similar to those in FIGS. 11A and 11B are omitted here. The first dielectric layer 24 comprises a plurality of dielectric islands 24a. The first conductive layer 26 fill the trenches of the first dielectric layer 24 to completely surround the dielectric islands 24a, thus achieving a lattice form.

FIG. 13A is a cross-section of the first conductive layer 26 patterned as independent plugs. FIG. 13B is a top view of the first conductive layer 26 shown in FIG. 13A. Elements similar to those in FIGS. 11A and 11B are omitted here. The first dielectric layer 24 comprises a plurality of via holes. The first conductive layer 26 fills the via holes of the first dielectric layer 24 to form a plurality of independent plugs 26. Additionally, the independent plugs 26 can be electrically connected to each other through a third conductive layer 38 underlying the plugs 26.

Other interconnections underlying the first conductive layer 26 may also be modified to have a ring, lattice, island, or solid profile as disclosed in FIGS. 3A~3C.

Second Example

Based on the passivation opening design rule, the first conductive layer 26 may be further modified to have a solid form.

FIG. 14A is a cross-section of the first conductive layer 26 patterned as a solid form. FIG. 14B is a top view of the first conductive layer 26 shown in FIG. 14A. Elements similar to those in FIGS. 11A and 11B are omitted here. The first conductive layer 26 fills a large-size trench of the first dielectric layer 24 to become a solid form. In addition, other interconnections underlying the

first conductive layer 26 may be modified to have ring, lattice, island, or solid profiles as disclosed in FIGS. 3A~3C.

Third Example

Based on the passivation opening design rule, the first conductive layer 26, the conductive pad 32 or a combination thereof may be further modified to have various profiles including quadrilateral, circular and polygonal profiles as described in FIGS. 4A~4F and FIGS. 5A~5F. Features similar to those in FIGS. 4~5 are omitted here.

Fourth Example

Based on the passivation opening design rule, the first conductive layer 26, the conductive pad 32 or a combination thereof may be further modified with at least one corner cut portion as described in FIGS. 6A and 6B. Features similar to those in FIGS. 6A and 6B are omitted here.

Fifth Example

Based on the passivation opening design rule, the first conductive layer 26, the conductive pad 32 or a combination thereof may be further modified with a marking notch as described in FIGS. 7A and 7B and FIGS. 8A and 8B. Features similar to those in FIGS. 7~8 are omitted here.

Sixth Example

Based on the passivation opening design rule, a circuit under pad (CUP) scheme 50 can be provided under an extension portion 26a the first conductive layer 26 as described in FIGS. 9~10. Features similar to those in FIGS. 9~10 are omitted here.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to

be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.